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(54) Semiconductor antifuse structure and method

(57) A method for forming an array of antifuse structures on a semiconductor substrate which previously has had CMOS devices fabricated thereupon up to first metallization. A fuse structure is formed as a sandwich by successively depositing a bottom layer of TiW, a layer of amorphous silicon, and a top layer of TiW. The amorphous silicon is formed in an antifuse via formed in a dielectric layer covering the bottom layer of TiW. First metallization is deposited and patterned over the top

layer of TiW. An intermetal dielectric layer is formed over the fuse array and second metal conductors are formed thereupon. An alternative embodiment includes forming an oxide sidewall spacer around the periphery of an antifuse structure. Connection resistance to the bottom layer of TiW is lowered by using a number of vias between the second-metal conductors and the bottom layer of TiW in a row of an array of antifuse devices.

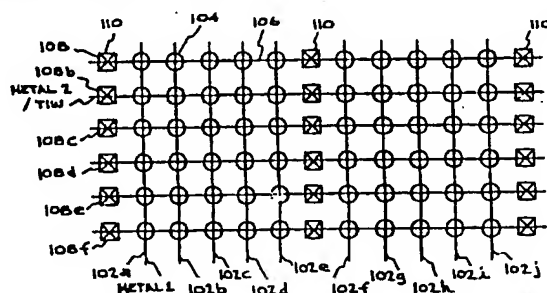


FIG. 2A



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 95 10 7360

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
D,A	STOPPER H.: "A Wafer with Electrically Programmable Interconnections" IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE, vol. 28, February 1985, CORAL GABLES FLORIDA, US, pages 268-269, XP002046003 * the whole document *	1,4-7	H01L23/525
A	US 4 748 490 A (HOLLINGSWORTH DEEMS R) 31 May 1988 * column 2, line 59 - column 4, line 60; figures 1-3 *	1,5-7	
A	US 4 569 121 A (LIM SHELDON C P ET AL) 11 February 1986 * column 5, line 4 - column 6, line 42; figures 8-10 *	1,4-7	
A	GB 2 066 566 A (ENERGY CONVERSION DEVICES INC) 8 July 1981 * page 4, line 20 - line 102; figures 1,2 * * page 5, line 70 - line 99; figure 5 *	1,4,6	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A	WO 85 03599 A (NCR CO) 15 August 1985 * page 5, line 27 - page 7, line 36; figures 1-9 *	1,6	
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 7 November 1997	Examiner Le Minh, I
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document</p>			

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